accordance with one embodiment of the present invention. The package 10 has a semiconductor device 12, a dielectric substrate 14, and a ball grid array (BGA) 16. The semiconductor device 12 has an integrated circuit (not shown). A suitable adhesive 18 may be used to secure the semiconductor device 12 to the substrate 14. The semiconductor device 12 and the substrate 14 may be diced from a layered wafer-tape assembly 20 as described in more detail below in connection with FIG. 2. The dicing process causes the 22 of the substrate 14 to be aligned with edges 24 of the semiconductor device 12.

B1

Page 5, the paragraph beginning at line 30 through page 6, line 9:

The ball grid array 16 may be used to mechanically and electrically connect the package 10 to a circuit board (not shown). Wire bonds 26, bond pads 28, circuit traces 30, and ball pads 32 may be used to provide electrical communication between the semiconductor device 12 and the ball grid array 16. The wire bonds 26 extend through a slot-shaped opening 34. The traces 30 may be printed on a top surface 36 of the substrate 14 (before the semiconductor device 12 is adhered to the substrate 14). An insulative solder mask 38 extends over the traces 30. The mask 38 has openings 40 for receiving the individual balls of the ball grid array 16. A screen printing process may be used to apply the solder mask 38 as a paste to the entire surface of the substrate 14 except for the slot-shaped opening 34 and the ball pads 32. The wire bonds 26 and the bond pads 28 may be encapsulated in a suitable liquid encapsulant 42.

B2

Page 8, the paragraph beginning at line 11 through line 19:

The package 60 may be singulated from a wafer-tape assembly of the type shown in FIGS. 2 and 3. With respect to the FIG. 4 embodiment, however, a metal sheet (not shown) is located between the wafer 50 and the tape 52 before the dicing operation. The metal layer 62 is singulated from the metal sheet when the assembly is

B3

diced (after full wafer testing). The metal sheet may cover all of the semiconductor devices 12 in the wafer 50. The dicing operation causes edges 64 of the metal layer 62 to be aligned with edges 22, 24 of the substrate 14 and the semiconductor device 12. As in the embodiment of FIGS. 1-3, plural packages 60 may be tested and burned-in before they are singulated from the layered assembly.

B3

Page 9, the paragraph beginning at line 8 through line 16:

As shown in FIG. 6, a solder mask 82 extends over the exterior traces 78. The mask 82 has openings 40 aligned with the ball pads 32 for receiving the solder balls and/or conductive bumps of the ball grid array 16. The mask 82 extends all the way across the central portion 84 of the substrate 72. Similarly to the FIGS. 1-5 embodiments, the package 70 shown in FIG. 6 may be singulated from a wafer-tape assembly. That is, the substrate 72 may be diced from a larger sheet of dielectric material (not shown) after the sheet is attached to a wafer 50, and after all of the packages 70 are tested and burned-in. The dicing operation causes edges 24 of the semiconductor device 12 to be aligned with edges 86 of the substrate 72.

B4

Page 9, the paragraph beginning at line 18 through line 26:

If desired, a metal layer 90 (FIG. 7) may be attached to the semiconductor device 12 by a suitable adhesive 92. The thickness of the metal layer 90 may be in the range of from about 0.13 millimeters to about 0.25 millimeters. The metal layer 90 may operate as a heat sink or heat spreader to thermally stabilize the semiconductor device 12. In addition, the metal layer 90 may provide stiffness for package 94. The metal layer 90 is preferably attached to the semiconductor device 12 before the device 12 is singulated from the wafer 50. This way, the metal layer 90 provides stiffness to the wafer-tape assembly prior to and during the dicing operation. The dicing operation

B5